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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,196	03/11/2004	Todd R. Abbott	MI22-2447	8742

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WELLS ST. JOHN P.S.
601 W. FIRST AVENUE, SUITE 1300
SPOKANE, WA 99201

EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/800,196	ABBOTT ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-13* is/are allowed.

6)☒ Claim(s) *14-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/17/05,6/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 14, 16, 17, 18, 20, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Goth et al. (U.S. 4,549,927).

Regarding claim 14, Goth et al. teaches a method of forming a semiconductor structure, comprising:

- providing a semiconductor material having a trench extending therein (**14** in Fig. 1);
- forming a first electrically insulative material within a bottom portion of the trench to partially fill the trench, the partially filled trench having a sidewall comprising the semiconductor material (polyimide film **20** in Fig. 4);
- incorporating the semiconductor material of the sidewall into a silicide, the silicide being a line extending along the trench (platinum silicide layer **25** in Fig. 8; column 6, lines 36-60); and
- filling the trench with a second electrically insulative material to cover the silicide (polyimide layer **26** in Fig. 8).

Regarding claim 16, Goth et al. teaches the method of claim 14, and further teaches forming a metal-containing layer over the substrate (platinum silicide layer **25** in Fig. 8), within the partially filled trench and along the sidewall; and forming the silicide

from metal of the metal-containing layer by reacting metal from the metal-containing layer with the semiconductor material of the sidewall (column 6, lines 36-60).

Regarding claim 17, Goth et al. teaches the method of claim 14, and further teaches teaches forming a metal-containing layer over the substrate (platinum silicide layer **25** in Fig. 8), within the partially filled trench and along the sidewall; and forming the silicide from metal of the metal-containing layer by reacting some of the metal from the metal-containing layer with the semiconductor material of the sidewall, some of the metal of the metal-containing layer not reacting to form the silicide; and removing the unreacted metal of the metal-containing layer (column 6, lines 36-60).

Regarding claim 18, Goth et al. teaches the method of claim 14, and further teaches that the semiconductor material comprises a first doped region (p- region **11** in Fig. 1) and a second doped region (n+ region **12** in Fig. 1) over the first doped region; one of the first and second doped regions is a p-type region and the other is an n-type region; the trench extends entirely through the second doped region and has a portion extending within the first doped region (Fig. 1); and the first electrically insulative material entirely fills the portion of the trench that is within the first doped region (Fig 2).

Regarding claim 20, Goth et al. teaches the method of claim 18, and further teaches that the first doped region is the p-type region (Fig. 1).

Regarding claim 21, Goth et al. teaches the method of claim 14, and further teaches that the first and second electrically insulative materials are the same as one another in chemical composition (polyimide layers **20** and **26**).

Claims 14-17 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (U.S. 6,133,105).

Regarding claim 14, Chen et al. teaches a method of forming a semiconductor structure, comprising:

- providing a semiconductor material having a trench extending therein (**206** in Fig. 2A);
- forming a first electrically insulative material within a bottom portion of the trench to partially fill the trench, the partially filled trench having a sidewall comprising the semiconductor material (oxide layer **208a** in Fig. 2B);
- incorporating the semiconductor material of the sidewall into a silicide, the silicide being a line extending along the trench (**236** in Fig. 2F; column 4, lines 36-62); and

filling the trench with a second electrically insulative material to cover the silicide (dielectric layer **238** in Fig. 2F covers the silicide until contact hole **242** is formed).

Regarding claim 15, Chen et al. teaches the method of claim 14, and further teaches incorporating the silicide line into a bitline (column 4, lines 59-64).

Regarding claim 16, Chen et al. teaches the method of claim 14, and further teaches forming a metal-containing layer over the substrate, within the partially filled trench and along the sidewall; and forming the silicide from metal of the metal-containing layer by reacting metal from the metal-containing layer with the semiconductor material of the sidewall (column 4, lines 36-62).

Regarding claim 17, Chen et al. teaches the method of claim 14, and further teaches teaches forming a metal-containing layer over the substrate, within the partially filled trench and along the sidewall; and forming the silicide from metal of the metal-containing layer by reacting some of the metal from the metal-containing layer with the semiconductor material of the sidewall, some of the metal of the metal-containing layer not reacting to form the silicide; and removing the unreacted metal of the metal-containing layer (column 4, lines 36-62).

Regarding claim 22, Chen et al. teaches the method of claim 14, and further teaches that said sidewall is one of a pair of opposing sidewalls within the partially filled trench; the silicide line is a first silicide line; semiconductor material of the other said pair of opposing sidewalls is incorporated into a silicide to form a second silicide line extending along the trench; and the second silicide line is spaced from the first silicide line (see silicide lines **236** in Fig. 2F).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goth et al. (U.S. 4,549,927) in view of Wolf (Silicon Processing for the VLSI Era, vol. 2, 1990).

Regarding claim 19, Goth et al. teaches the method of claim 18, but does not teach that the first doped region is the p-type region. Rather, Goth et al. teaches an npn bipolar transistor having an n-doped first region.

Wolf teaches that it is advantageous to incorporate both npn and pnp transistors into a circuit (paragraph bridging pages 557 and 558).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a first region of p-type material and thereby incorporate a pnp bipolar transistor. The motivation for doing so at the time of the invention would have been that circuits that contain both npn and pnp transistors offer the potential of providing the high-speed performance of bipolar logic gates, but dissipate little standby power, as taught by Wolf (paragraph bridging pages 557 and 558).

Allowable Subject Matter

Claims 1-13 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: Prior art does not teach or suggest, in combination with the other claimed limitations, that the silicide is within the second doped semiconductor region, and not within the first doped semiconductor region. Goth et al. (U.S. 4,549,927) teaches a method similar to the invention as claimed in claim 1, but forms a silicide layer extending over the entire height of a trench sidewall so that the silicide is within both doped semiconductor regions.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gratz (U.S. 6, 717,205) teaches a trench extending through first (n-type) and second (p-type) doped semiconductor regions with a metal silicide layer lining the upper sidewalls of the trench, but the silicide is deposited on an insulating layer, not formed by reacting a metal-containing layer with the semiconductor of the sidewalls.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800